

1     **CLAIMS:**

2             1.     A capacitor comprising:

3                 a substrate node location;

4                 a first container joined with the node location and having an  
5     opening defining a first interior area;

6                 a second container joined with the node location and having an  
7     opening defining a second interior area, the areas being spaced apart  
8     from one another in a non-overlapping relationship; and

9                 a dielectric layer and a conductive capacitor electrode layer  
10     disposed operably proximate the first and second containers.

11  
12             2.     The capacitor of claim 1, wherein the containers are  
13     elongate.

14  
15             3.     The capacitor of claim 1, wherein the containers are  
16     elongate and extend along generally parallel central axes.

17  
18             4.     The capacitor of claim 1, wherein the openings are generally  
19     circular in shape.

20  
21             5.     The capacitor of claim 1, wherein the containers are  
22     generally tubular in construction.

1           6.    The capacitor of claim 1, wherein the capacitor comprises  
2   only two conductive capacitor electrodes separated by a dielectric region.  
3

4           7.    A capacitor comprising:

5           a substrate node location;

6           a first elongate container joined with the node location and  
7   extending away therefrom along a first central axis;

8           a second elongate container joined with the node location and  
9   extending away therefrom along a second central axis which is different  
10   and spaced apart from the first central axis; and

11          a dielectric layer and a conductive capacitor electrode layer  
12   disposed operably proximate the first and second containers.  
13

14          8.    The capacitor of claim 7, wherein the first and second  
15   central axes are generally parallel.  
16

17          9.    The capacitor of claim 7, wherein the containers are  
18   generally cylindrical in shape.  
19

20          10.   The capacitor of claim 7, wherein one of the containers is  
21   generally cylindrical in shape.  
22  
23  
24

1        11. The capacitor of claim 7, wherein one of the containers is  
2 generally cylindrical in shape, and portions of the first and second axes  
3 are generally parallel.

4  
5        12. The capacitor of claim 7, wherein each container comprises  
6 an opening away from the node location which is generally circular in  
7 shape.

8  
9        13. The capacitor of claim 7, wherein the capacitor comprises  
10 only two conductive capacitor electrodes separated by a dielectric region.

11  
12        14. A capacitor comprising a pair of capacitor electrodes  
13 separated by a capacitor dielectric layer, the electrodes collectively  
14 comprising first and second non-laterally-overlapping containers.

1           15. DRAM circuitry comprising:

2           a substrate node location;

3           a conductive layer of material disposed over and in electrical  
4 communication with the substrate node location, the layer of material  
5 having an outer surface with a first region and a second region spaced  
6 apart from the first region;

7           a first container formed over and in electrical communication with  
8 the first region;

9           a second container formed over and in electrical communication  
10 with the second region; and

11          a dielectric layer and a conductive capacitor electrode layer  
12 disposed operably proximate the first and second containers.

13  
14          16. The DRAM circuitry of claim 15, wherein the first and  
15 second containers are generally elongate.

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17          17. The DRAM circuitry of claim 15, wherein the first and  
18 second containers are generally elongate and extend along respective  
19 central axes, and wherein each container comprises a container portion  
20 having a generally circular transverse cross section.

21  
22          18. The DRAM circuitry of claim 15, wherein the first and  
23 second containers are generally elongate and extend along respective  
24 central axes which are generally parallel with one another.

1           19. The DRAM circuitry of claim 15, wherein the first and  
2 second containers define container volumes which are substantially the  
3 same in magnitude.  
4

5           20. The DRAM circuitry of claim 15, wherein the first and  
6 second containers are generally elongate and extend along respective  
7 central axes which are generally parallel with one another, and wherein  
8 each container comprises a container portion having a generally circular  
9 transverse cross section.  
10

11           21. The DRAM circuitry of claim 15, wherein the first and  
12 second containers are generally elongate and extend along respective  
13 central axes which are generally parallel with one another, and wherein  
14 each container comprises a container portion having a generally circular  
15 transverse cross section, and wherein the first and second containers  
16 define container volumes which are substantially the same in magnitude.  
17

18           22. The DRAM circuitry of claim 15, wherein the first  
19 container, the second container, the dielectric layer and the capacitor  
20 electrode layer comprise only two conductive capacitor electrodes  
21 separated by a dielectric region.  
22  
23  
24

1           23.    DRAM circuitry comprising:  
2           a substrate having first and second spaced apart node locations;  
3           a first storage capacitor in electrical communication with the first  
4   node location and comprising first and second containers;  
5           a second storage capacitor in electrical communication with the  
6   second node location and comprising third and fourth containers,  
7   wherein the first, second, third, and fourth containers define container  
8   volumes which are discrete and separated from one another; and  
9           a dielectric layer and conductive capacitor electrode layer disposed  
10   operably proximate the first and second containers.

11  
12           24.    The DRAM circuitry of claim 23, wherein the containers are  
13   generally elongate.

14  
15           25.    The DRAM circuitry of claim 23, wherein the containers are  
16   generally elongate and extend along respective central axes at least two  
17   of which being generally parallel.

18  
19           26.    The DRAM circuitry of claim 23, wherein the containers are  
20   generally elongate, and extend along respective central axes which are  
21   generally parallel with one another.

1           27.    The DRAM circuitry of claim 23, wherein the containers are  
2   generally elongate and extend along respective central axes, and wherein  
3   each container comprises a respective portion which has a generally  
4   circular transverse cross-section.

5  
6           28.    The DRAM circuitry of claim 23, wherein the containers are  
7   generally elongate and cylindrical in shape, and extend along respective  
8   central axes.

9  
10          29.    The DRAM circuitry of claim 23, wherein the container  
11   volumes are substantially the same in magnitude.

12  
13          30.    The DRAM circuitry of claim 23, wherein the containers are  
14   generally elongate and extend along respective central axes which are  
15   generally parallel with one another, and wherein each container  
16   comprises a respective portion which has a generally circular transverse  
17   cross-section, and further wherein the container volumes are substantially  
18   the same in magnitude.

19  
20          31.    The DRAM circuitry of claim 23, wherein the first, second,  
21   third and fourth containers, the dielectric layer and the conductive  
22   capacitor electrode layer comprise different respective capacitors having  
23   only two conductive capacitor electrodes separated by a dielectric region.  
24

1           32. A method of forming a capacitor comprising:  
2           forming a first container joined with a substrate node location, the  
3           first container having an opening defining a first interior area;  
4           forming a second container joined with the node location, the  
5           second container having an opening defining a second interior area, the  
6           areas being spaced apart from one another in a non-overlapping  
7           relationship; and  
8           forming a dielectric layer and a conductive capacitor electrode  
9           layer disposed operably proximate the first and second containers.

10  
11           33. The method of claim 32, wherein the forming of the first  
12           and second containers comprises forming generally elongate first and  
13           second containers.

14  
15           34. The method of claim 32, wherein the forming of the first  
16           and second containers comprises forming generally elongate first and  
17           second containers which extend along individual central axes which are  
18           generally parallel with one another.

19  
20           35. The method of claim 32, wherein the forming of the first  
21           and second containers comprises forming the openings to be generally  
22           circular.



1           36. The method of claim 32, wherein the forming of the first  
2 and second containers comprises forming generally elongate first and  
3 second containers having openings which are generally circular.

4  
5           37. The method of claim 32 further comprising forming said  
6 capacitor to comprise only two conductive capacitor electrodes separated  
7 by a dielectric region.

8  
9           38. A method of forming a capacitor comprising:  
10 forming a first elongate container joined with a substrate node  
11 location and extending away therefrom along a first central axis;  
12 forming a second elongate container joined with the node location  
13 and extending away therefrom along a second central axis which is  
14 different and spaced apart from the first central axis; and  
15 forming a dielectric layer and a conductive capacitor electrode  
16 layer disposed operably proximate the first and second containers.

17  
18           39. The method of claim 38, wherein the forming of the first  
19 and second elongate containers comprises forming the containers to have  
20 central axes which are generally parallel with one another.

21  
22           40. The method of claim 38, wherein the forming of the first  
23 and second elongate containers comprises forming the containers to be  
24 generally cylindrical in shape.

1           41. The method of claim 38, wherein the forming of the first  
2 and second elongate containers comprises forming the containers to be  
3 generally cylindrical in shape and have central axes which are generally  
4 parallel with one another.

5  
6           42. The method of claim 38 further comprising forming said  
7 capacitor to comprise only two conductive capacitor electrodes separated  
8 by a dielectric region.

9  
10          43. A method of forming DRAM circuitry comprising:  
11           forming a conductive layer of material disposed over and in  
12 electrical communication with a substrate node location, the layer of  
13 material having an outer surface with a first region and a second region  
14 spaced apart from the first region;  
15           forming a first container over and in electrical communication with  
16 the first region;  
17           forming a second container over and in electrical communication  
18 with the second region; and  
19           forming a dielectric layer and a conductive capacitor electrode  
20 layer disposed operably proximate the first and second containers.

21  
22          44. The method of claim 43, wherein the forming of the first  
23 and second containers comprises forming the containers to be generally  
24 elongate.

1           45. The method of claim 43, wherein the forming of the first  
2 and second containers comprises forming the containers to be generally  
3 elongate and extend along respective central axes which are generally  
4 parallel with one another.

5  
6           46. The method of claim 43, wherein the forming of the first  
7 and second containers comprises forming the containers to have volumes  
8 which are substantially the same in magnitude.

9  
10          47. The method of claim 43, wherein the forming of the first  
11 and second containers comprises forming the containers to be generally  
12 elongate and have volumes which are substantially the same in  
13 magnitude.

14  
15          48. The method of claim 43, wherein the forming of the first  
16 container, the second container, the dielectric layer, and the conductive  
17 capacitor electrode comprises forming a capacitor comprising only two  
18 conductive capacitor electrodes separated by a dielectric region.

1           49. A method of forming DRAM circuitry comprising:  
2           providing a substrate having first and second spaced apart node  
3           locations;  
4           forming a first storage capacitor in electrical communication with  
5           the first node location and comprising first and second containers;  
6           forming a second storage capacitor in electrical communication  
7           with the second node location and comprising third and fourth  
8           containers, wherein the first, second, third, and fourth containers define  
9           container volumes which are discrete and separated from one another;  
10          and  
11          forming a dielectric layer and conductive capacitor electrode layer  
12          disposed operably proximate the first and second containers.

13  
14          50. The method of claim 49, wherein the forming of the first  
15          and second storage capacitors comprises forming individual containers to  
16          be generally elongate.

17  
18          51. The method of claim 49, wherein the forming of the first  
19          and second storage capacitors comprises forming individual containers to  
20          be generally elongate and extend along respective central axes at least  
21          two of which being parallel.

1           52. The method of claim 49, wherein the forming of the first  
2 and second storage capacitors comprises forming individual containers to  
3 be generally elongate and extend along respective central axes which are  
4 parallel with one another.

5  
6           53. The method of claim 49, wherein the forming of the first  
7 and second storage capacitors comprises forming individual containers to  
8 be generally elongate and cylindrical in shape and extend along  
9 respective central axes which are parallel with one another.

10  
11           54. The method of claim 49, wherein the forming of the first  
12 storage capacitor, the second storage capacitor, the dielectric layer and  
13 the conductive capacitor electrode layer comprises forming different  
14 respective capacitors comprising only two conductive capacitor electrodes  
15 separated by a dielectric region.